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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,271	10/30/2003	Boon Seong Ang	200300182-1	1610

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,271	ANG ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *40 and 41* is/are allowed.

6)☒ Claim(s) *1-8,20,22-24,29-33 and 36-39* is/are rejected.

7)☒ Claim(s) *9-19,21,25-28,34 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/30/03*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

Specification

The disclosure is objected to because of the following informalities: On page 1, line 4, U.S. Application No. is missing. Appropriate correction is required.

Claim Objections

Claim 4 is objected to because of the following informalities: on lines 4-5, the clause, "a logic element" should be deleted because it is redundant. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 20, 22-24, 29-33, and 36-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Iadanza (US 5,651,013).

Regarding claim 1, Iadanza discloses, at least in Figs. 2, 4 and 5, a reconfigurable device comprising:

tiles (20 in Figs 2, 4) each comprising a circuit (68 in Fig. 4); and

an interconnect architecture (50) coupled to the circuit of each tile, the interconnect architecture comprising switches (100) and registers (120, 122) such that in operation some of the switches route a signal (52 or 62) from a first tile (20 shown in Fig. 4) to a second tile (adjacent 20 shown in Fig. 2) along the interconnect architecture and further such that in

operation at least two of the registers (120, 122) consecutively latch the signal at a time interval (A, B, C or ALT CLOCK 56) of no more than a repeating time period.

Regarding claim 2, Iadanza discloses, at least in Figs. 2, 4 and 5, that the repeating time period comprises a clock cycle period (col. 3, lines 20+).

Regarding claim 3, Iadanza discloses, at least in Figs. 2, 4 and 5, that the repeating time period comprises a multiple of a clock cycle period (col. 3, lines 20+)..

Regarding claim 4, Iadanza discloses, at least in Figs. 2, 4 and 5, that the circuit of one of the tiles comprises elements selected from a group consisting of a look-up table, an arithmetic unit, a multiplier, a reconfigurable interconnect, a memory block, a content addressable memory, a logic element (68), a specialized functional unit, and an other circuit element (64, 66).

Regarding claim 5, Iadanza discloses, at least in Figs. 2, 4 and 5, that the tiles comprise heterogeneous tiles (20 is inherently programmable to be different than other 20).

Regarding claim 6, Iadanza discloses, at least in Figs. 2, 4 and 5, that the tiles comprise homogeneous tiles (20 is inherently programmable to be identical to other 20).

Regarding claim 7, Iadanza discloses, at least in Figs. 2, 4 and 5, that the interconnect architecture further comprises data interchanges (66).

Regarding claim 8, Iadanza discloses, at least in Figs. 2, 4 and 5, that the data interchanges couple the interconnect architecture to the circuits of the tiles (68).

Regarding claim 20, Iadanza discloses, at least in Figs. 2, 4 and 5, that the data interchange comprises a plurality of the switches (66).

Regarding claim 22, Iadanza discloses, at least in Figs. 2, 4 and 5, that the interconnect architecture further comprises communication links (60 in Figs. 4, 5) coupling the data interchanges.

Regarding claim 23, Iadanza discloses, at least in Figs. 2, 4 and 5, that a length of each of the communication links (60) allows the signal to traverse the communication link within the repeating time period (A, B, C, or ALT CLOCK).

Regarding claim 24, Iadanza discloses, at least in Figs. 2, 4 and 5, a first communication link couples a first data interchange (66 of 1st 20) to a second data interchange (64 of 2nd 20).

Regarding claim 29, Iadanza discloses, at least in Figs. 2, 4 and 5, that each tile (20) comprises a mini-tile (68).

Regarding claim 30, Iadanza discloses, at least in Figs. 2, 4 and 5, that each tile comprises a plurality of mini-tiles (64, 68, 50, 66).

Regarding claim 31, Iadanza discloses, at least in Figs. 2, 4 and 5, that one of the mini-tile comprises a portion of the circuit (68) of one of the tiles.

Regarding claim 32, Iadanza discloses, at least in Figs. 2, 4 and 5, that each mini-tile (64, 68, 66) couples to the 2 interconnect architecture (50).

Regarding claim 33, Iadanza discloses, at least in Figs. 2, 4 and 5, that the interconnect architecture (50) further comprises data interchanges coupling the interconnect architecture to the mini-tiles.

Claims 36-39 are essentially the same in scope as apparatus claims as discussed above and are rejected similarly.

Allowable Subject Matter

Claims 40 and 41 are allowed.

Claims 9-19, 21, 25-28, 34-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER